

COGITO: Runtime Code Generation to Secure Devices

8emes rencontres de la communauté française de
compilation – Nice

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July 3, 2014

COGITO

Domain

Runtime code generation

... for security purposes in embedded systems, mainly against physical attacks

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Objectives: explore the use of runtime code generation as a means to secure embedded systems against physical attacks

How? deGoal:

- runtime code generation and code optimizations
- suitable for constrained embedded systems:
 - fast code generation
 - within tiny memory footprints: works on TI's Launchpad MSP430 (512 B RAM)

This talk is about:

- 1 An overview of security issues – aka physical security of embedded systems for dummies
... and how code polymorphism is likely to bring new solutions
- 2 A practical solution to achieve code polymorphism for security: deGoal
 - overview of deGoal
 - modification for security purposes
 - demo time



- Project coordination
 - Bringing the deGoal framework
 - Compilation & runtime code generation
-
- Scientific coordination
 - Security analysis
 - Physical attacks and software countermeasures
 - JavaCards
-
- Security analysis
 - Physical attacks, HW/SW countermeasures
 - Experimental validation

Public website

www.cogito-anr.fr

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- 2 Code polymorphism as a proposal to improve physical security in embedded systems
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 - Introduction to deGoal
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An attack is usually split between:

- 1 a **first step** attack:
 - global inspection of the target
 - identification of the security components involved (HW/SW)
 - identification of weaknesses
- 2 a **second step** attack:
 - focused attack
 - on an identified potential weakness

- **Reverse engineering**
 - HW inspection: decapsulation, abrasion, chemical etching, memory extraction, etc.
 - SW inspection: debug, memory dumps, code analysis, etc.
- **Side channel attacks:** SPA (Simple Power Analysis), DPA (Differential –), CPA (Correlation –)...
 - Electromagnetic analysis
 - Power analysis
 - Acoustic analysis
 - Timing attacks
- **Fault injection attacks**
 - under/over voltage drops
 - iom / laser beam, optical illumination
 - glitch attacks
 - ...

- Reverse engineering

- HW inspection: decapsulation, abrasion, chemical etching, memory

e)

SPA on AES [Kocher, 2011]:

- S'

0.5 1 1.5 2 2.5

- Side channel

CPA (

- E

- P

- A

- T

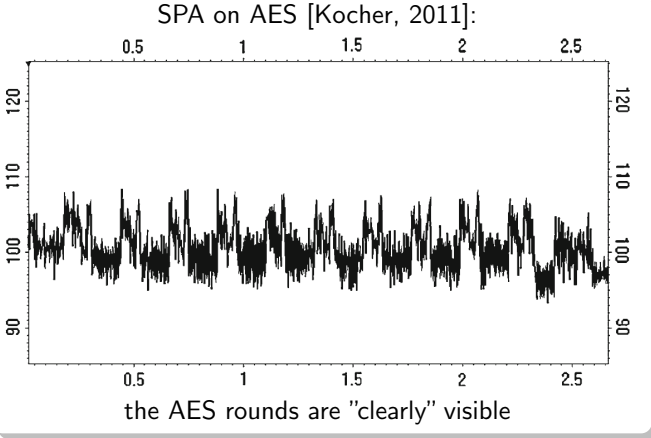
- Fault

- ui

- io

- gl

- ..



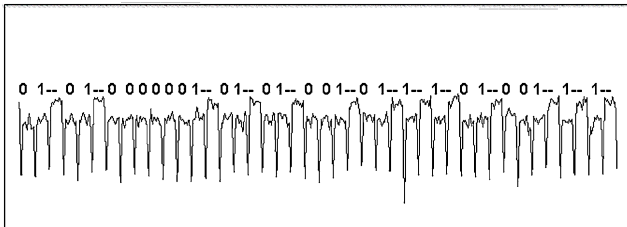
- Reverse engineering

- HW inspection: decapsulation, abrasion, chemical etching, memory extraction, etc.

- SPA on RSA [Kocher, 2011]:

- Side channel attacks (CPA)

- Electromagnetic (EM)
- Power (P)
- Acoustic (A)
- Thermal (T)



ifferential -),

- Fault

- Direct access to key's contents:
- bits 0 = square
- bits 1 = square + mul
- ...

DPA on AES:

- 1 get n traces from the target, using selected clear inputs
- 2 compute intermediate values for each input, for each possible key values
- 3 compute {power/EM/timing...} estimation from the intermediate values
- 4 correlate with the measurement traces

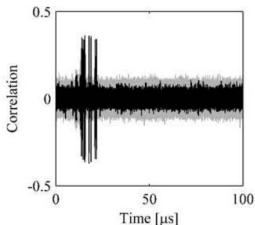


Figure 6.3. All rows of R . Key hypothesis 225 is plotted in black, while all other key hypotheses are plotted in gray.

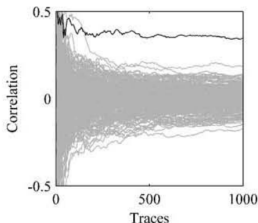


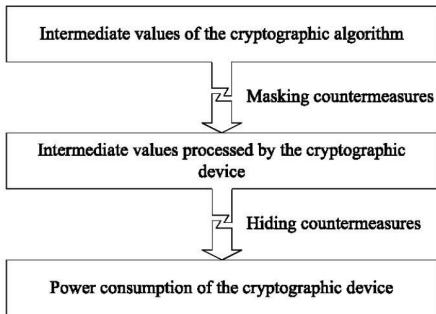
Figure 6.4. The column of R at 13.8 μ s for different numbers of traces. Key hypotheses 225 is plotted in black.

[Mangard, 2007]

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Hiding and masking decorrelate data processing from power consumption



Hiding: remove the data dependency of the power consumption

Masking: randomize the intermediate values that are processed by the cryptographic device (vs. algorithmic intermediate values)

[Mangard, 2007]

Our proposal

Use **code polymorphism** to tackle the problem of **program contents** as an **invariant**

Definition

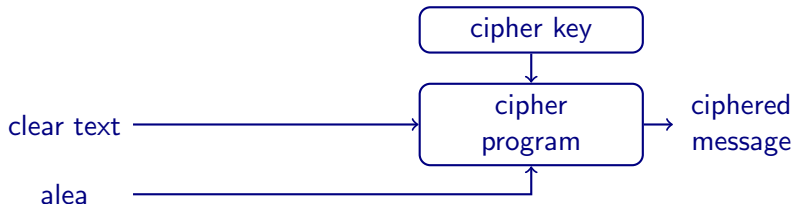
Regularly **changing the behaviour** of a (secured) component, **at runtime**, while maintaining **unchanged** its **functional properties**

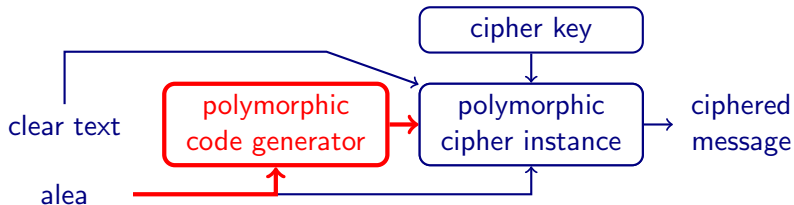
How?

- Generate secured (& polymorphic) functions **at runtime**
- ... thanks to a code generator
- Generate a new morphing each time it is necessary
 - security factor ω

What for ?

- SW reverse: more difficult
 - the secured code is not available before runtime
 - the secured code regularly changes its form
 - meta-analysis of the code generator?
- polymorphism changes **the spatial and temporal properties** of the secured code: side channel attacks fault attacks
- combine usual SW protections against 2nd step attacks

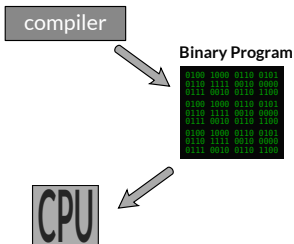




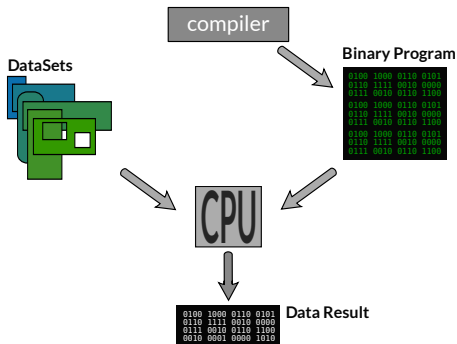
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- 1 Program performance: strong correlation to data
 - 2 Static compilation: no (or almost no) knowledge about the data
- deGoal is a tool that allows to design **complettes**
 - A complete is:
 - an *ad hoc* code generator that targets *one* kernel (\neq application)
 - aimed to be invocated at runtime

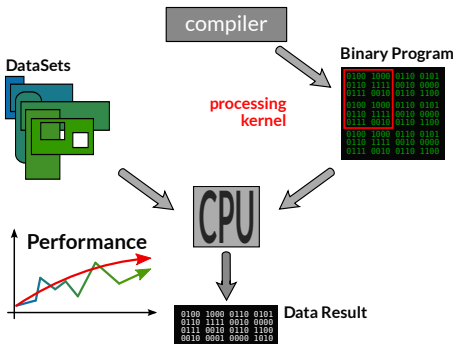
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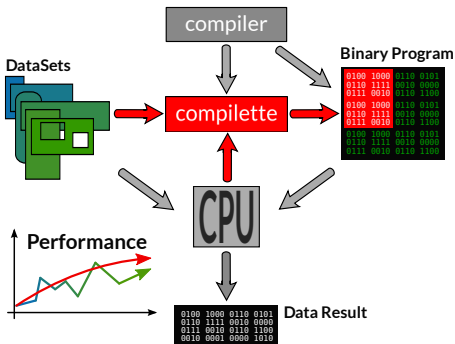
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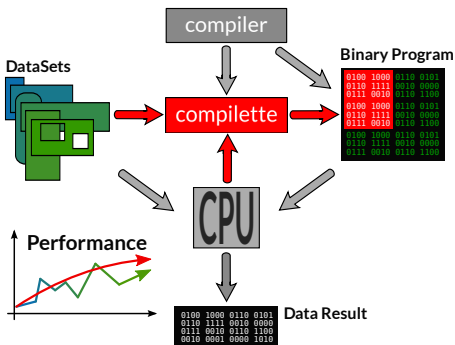


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Properties of complettes:

- low memory footprint
- high portability

Aim:

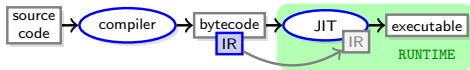
- Modify kernel's binary instructions
- according to the input data
- whenever needed at runtime

Static code versioning (e.g. C++ Templates)



- static compilation
- runtime: select executable
- memory footprint ++
- limited genericity
- runtime blindness

Dynamic compilation (JITs, e.g. Java Hotspot)



IR Intermediate Representation

- overhead ++
- memory footprint ++
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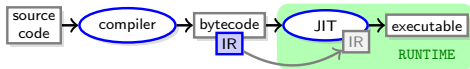
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Runtime code generation, with deGoal
A compilette is an ad hoc code generator, targeting one executable



- fast code generation
- memory footprint --
- **data-driven code generation**

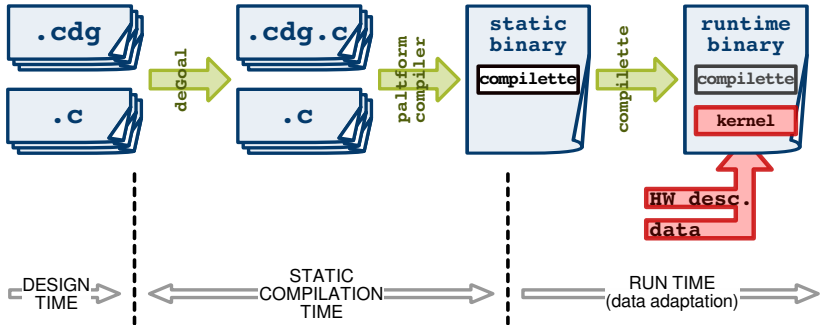
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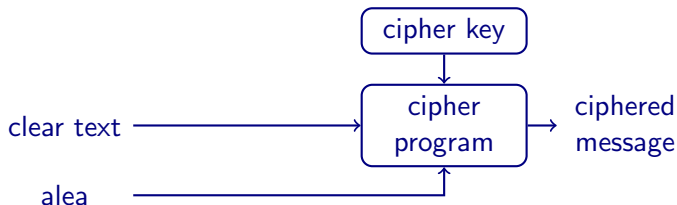
Development flow using deGoal

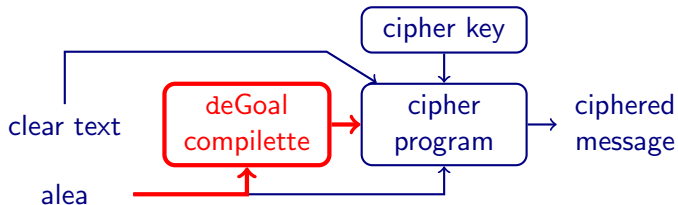


- ARM 32-bits, Thumb 1 & 2 (including NEON, VFP)
 - Cortex-A8 (beagleBoard), Cortex-A9 (snowball), Cortex-M3 (STM32 discovery – 8 kB RAM)
 - gem5 + McPAT
- MSP430 from Texas Instruments
 - TI's Launchpad (512 bytes only!), Zolertia
- MIPS 32 bits
- VLIW architectures: STxP70 (ST-Microelectronics), other VLIWs under NDA
- Nvidia GPUs (Cuda PTX assembly language)

It is the only tool for dynamic code generation able to target very small processors, up to 8-bit microcontrollers

Demonstrated for the **16-bit MSP430** with only **512 bytes of RAM**:
Software Acceleration of Floating-point Multiplication using Runtime Code Generation. C. Aracil & D. Couroussé. ICEAC 2013





deGoal runtime capabilities

Performed *in this order*:

- 1 register selection
- 2 instruction selection
- 3 instruction scheduling

What does it mean for COGITO:

- Portability to very small processors and secure elements
 - Limited memory consumption
 - Fast runtime code generation
- Ability to combine with hardware countermeasures
- Introduce alea during runtime code generation [1,2,3]
- Polymorphism: random generation of semantically equivalent sequences
 - random mapping to physical registers [1]
 - use of semantic equivalences [2]
 - instruction scheduling [3]
 - insertion of dummy operations [3]

Requirement: **writable program memory**

- Current practice:
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 - or in ROM (flash)

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- **Possible workarounds?**
 - Lower the side effects of this issue:
 - obfuscate the code generator with encryption
 - ...
 - Hardware design of a dedicated block ...

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The **code generator** itself must be secured against physical attacks

Out of the scope of this talk

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Target : $[B] = \alpha \times [A]$

```
typedef void (*fp)(int*);
int src[TABLE_LEN], dest[TABLE_LEN];

void vector_mul(int * A, int A_len, int alpha, int * B) {
    int i; for (i=0; i<A_len; i++) {
        B[i] = alpha * A[i];
    }
}

int main() {
    cdg_insn_t * code = CDGALLOC(ALLOC_LEN);
    compilette(code, src, vsize, alpha); /* code generation */

    fp kernel = (fp)code;
    kernel(dest); /* execution */

    PRINT("dest :");
    for (i = 0; i < vsize; ++i) { PRINT("%3d ", dest[i]); }
}
```

```
void compilette(cdg_insn_t* code, int * A_addr, int A_len, int alpha) {  
    # [  
    Begin code Prelude B_addr  
  
    Type ptr_t int 32  
    Type vint_t int 32 #(A_len)  
    Alloc vint_t v  
    Alloc ptr_t tmp  
  
    mv tmp, #(A_addr)  
    lw v, tmp  
    mul v, v, #(alpha)  
    sw B_addr, v  
    rtn  
  
    End  
    ] #;  
}
```

- non-polymorphic execution
- random register allocation
- instruction shuffling

Two positions opened !!

- Post-doc on COGITO
keywords: security, code generation,
[IoT]
- Embedded SW developer for MPSoCs
keywords: embedded, runtime SW,
code generation, parallelism



Thanks!



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list

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